PRAKALP-AN ANALOG DRIVE

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Abstract

In the present era, where technology is being improved and optimized at a rapid rate, understanding what the industries expect from graduates and preparing them for the same has become a very crucial task as it can aid in enhancing the performance of young engineers. In this regard, BVBCET has taken a step forward with an aim to bridge the gap that exists between the industry and academia in the field of VLSI by introducing "**PRAKALP**", a program collaborated by department of Electronics and Communication Engineering, BVBCET and Sankalp Semiconductors Private Limited, Hubli. Under PRAKALP, students interested to carry out Analog VLSI Design are selected through a screening test, trained on analog circuit design and are finally assigned industry level projects. These projects have fetched many prizes and have also resulted in many technical papers. Outstanding students get recruited by Sankalp Semiconductors.

Key words: Industry-Institute, Analog VLSI, Cadence contest.

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1 INTRODUCTION

Interaction between technical institutions and industry is the need of the hour. This will have a great impact on the engineering curriculum, it will expose engineering students to the industrial atmosphere and help subsequent placement of young graduating engineers in industries. There is a need to prepare engineering students for jobs in multinational companies and exposing them to new technologies and engineering methodologies. These objectives can only be achieved well by bridging the gap between industry and the academia.

Every institute aims at imparting best knowledge to its students and prepares them to be a part of multinational companies. To achieve this vision of the institutions it is necessary to expose the students to new technologies and engineering methodologies. Industrial exposure is the need of the hour.

It has also been observed that:

1) The number of students who continue higher studies in the field of VLSI is very less.

2) The numbers of VLSI companies are less as compared to software companies resulting in few opportunities in this field.

3) The surprisingly small number of placements in VLSI field is also due to poor fundamentals and technical knowledge of students in VLSI

4) The students are not exposed to industrial standards.

With an objective to overcome all the above mentioned limitations, BVBCET and Sankalp Semiconductors joined

hands in coming up with PRAKALP with the benefit of mutual help.

Its main objective is to drive analog through industry standard projects in analog VLSI.

In this regard students are trained in theory and practical, so that they are ready to implement these projects. The expected outcome would be in terms of placements in VLSI companies and pursuing higher studies in VLSI.

1.1 Prakalp Process

1. Screening test for students of 3rd sem, of ECE, IT and EEE branches. Questions were based on fundamentals of Analog Electronics, Electrical Circuits, Geometry and Aptitude.
2. Selection of students based on cut-off mark set in.
3. Training on fundamentals and advance topics of analog VLSI by senior students, faculty and Sankalp engineers.
4. Team formation, Project allocation, assignment of guide and Sankalp mentor.
5. Fortnight reviews (alternatively) by Sankalp mentors and dept. guides.
6. Performance/Project evaluation.

With an intention to drive analog VLSI, Prakalp in 2012 floated ten analog VLSI projects for the students of ECE, IE and E&E branches. Interested pre-final year and final year students in a batch of four started working on these projects. Each batch was assigned a mentor from a Sankalp along with the dept. guide. Required training to carry out the project was done by a senior students, faculty and Sankalp engineers.

The students were trained in the area of VLSI for 40 hours. Sessions were on fundamental courses like Analog, Circuits, Signals, Control engineering and VLSI. Sankalp engineers helped in exploring and mastering the simulation tool (cadence). Every fortnight reviews were conducted by Sankalp mentors along with Dept. guides. Five projects were implemented during their final year. The projects involved circuit design, simulation and layout. A paper presented in **Cadence Analog Design contest 2013, secured Runners-up prize**. A total of 133 entries from 45 Engineering institutes were narrowed down to 13 finalists by the expert committee. It was of great motivation to us.

The second batch of Prakalp (2013-14 final year batch) also underwent the same process of project implementation. Four projects on analog VLSI were implemented during their final year. **A paper published from this batch secured first place at BITS, Goa.**

With an objective of having full chip design experience to students, Prakalp started third batch in 2013 for 2nd year (2011-15 batch) students. During the vacation of 3rd semester, students were trained on fundamentals concepts of Analog Electronics, Signals and Systems, Circuit Theory for two weeks and in long term vacation of 4th semester one month training on Analog VLSI was given. Four hours of theory sessions in the morning and four hours of practical sessions were conducted by the senior students under the guidance of Prakalp coordinator. This batch had 4 full semesters to carry out the projects. This long duration involvement helped students to have in- depth understanding of the project. A project from this batch has been selected for final presentation in Cadence Design Contest.

Fourth batch of Prakalp started in 2014 again for 2nd year (2012-16) students. A written test consisting of basic subjective questions on network analysis and RC circuits was conducted to filter the interested and passionate students. This batch included two M.Tech students. A training session focusing on learning basics of VLSI as well as exploring the cadence ICFB tool was conducted for these students, thus a right proportion of learning theory and being able to correlate it practically was achieved. Training sessions were conducted by the senior Prakalp students, faculty of BVBCET and experts from Sankalp semiconductors Pvt. Ltd. This training went on for a month long duration and the feedback from the students reflected an overwhelming response. Again the projects were given to the students with an aim of full chip implementation. i.e., the students were exposed to the full design and layout cycle of the VLSI. The mentors from

Sankalp Semiconductor Pvt. Ltd. were assigned for each project. Regular interactions were conducted for the students with their respective mentors and valuable feedback was received.

Fifth batch of Prakalp commenced during Jan, 2015 for 3rd sem students of 2013-17 batch. One week training on RLC basics, Circuit analysis, MOS fundamentals was conducted during Jan, 2015. This time a 3 credit course on Analog Circuit Design was conducted for these students during June, 2015. Classes were conducted by s dept. faculty and Sankalp Engineers.

Continuous evaluation of this course was based on two minor exams, circuit simulations and course project implementation. Each of two students group was assigned a course projects, defined by Sankalp. The final evaluation is yet to happen. This course which was conducted during vacation of 4th semester gets reflected as a 7th semester elective.

2. CONCLUSION

This section analyses the outcome of the conducted program, and reflects upon some better practices relevant for engineering education. From the Prakalp 2nd batch, two students; 3rd batch six students got the direct recruitment opportunity, based on their performance of the execution of their Prakalp projects. An increase of 200 % can be observed from the previous mentioned batch, which attributes as a success of the Prakalp's 2nd batch. Several achievements have been accomplished by the students of this program. Some of the exceptional cases are

1) Runners place in Cadence™ Design Contest,2013 was secured by a team of 3 students from the 1st batch of Prakalp.

2) First place in paper presentation at BITS, Goa was secured by a team of 3 students of 2nd batch of Prakalp

3) Runners place in Cadence™ Design Contest,2015 was secured by a team of 2 students from the 3rd batch of Prakalp.

4) Paper presentation at VDAT, 2015

The Table no.1 below highlights the increase in number of the students interested to take up VLSI project and respective placements based on their performance, as part of this program.

Batch	Number of students	
	Appeared	Placed
2009-13	17	2
2010-14	20	2
2011-15	28	6
2012-16	32	4 (Under process)
2013-17	23	

Tab.1: No. of students per batch and respective recruitments.

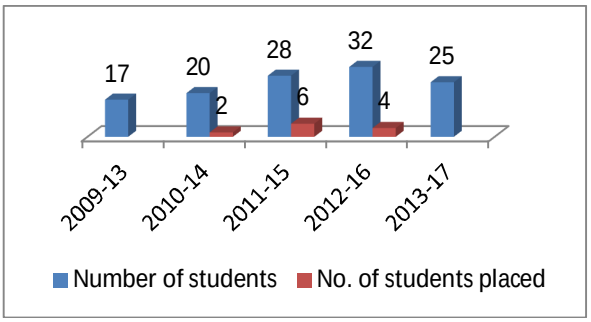

Fig. 1: No of students registered and recruited.

Good practices reflecting new trends in engineering education have come up in execution of

Prakalp program from the very beginning. Some of the salient practice features of this program are:

1. Industry is directly involved in the mini and major projects of the students. This has lead to quality projects, i.e., the projects being accomplished are closer to the industry level of execution.

2. Students involvement in training the juniors in the field of VLSI. This has created a feedback kind of environment wherein students contribute in making the junior understand what they have learnt. It gives them an opportunity to share their ideas and knowledge they have acquired.

3. Problem solving skills is found to have been increased among the students after the Prakalp program. Profound interest towards the Analog VLSI among the students is seen.

4. More number of students are ready to be the part of this ever growing mixed signal industry.

The recruitment of of all Prakalp students in VLSI domain is a big challenge, as very few core VLSI companies come for campus recruitment.

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